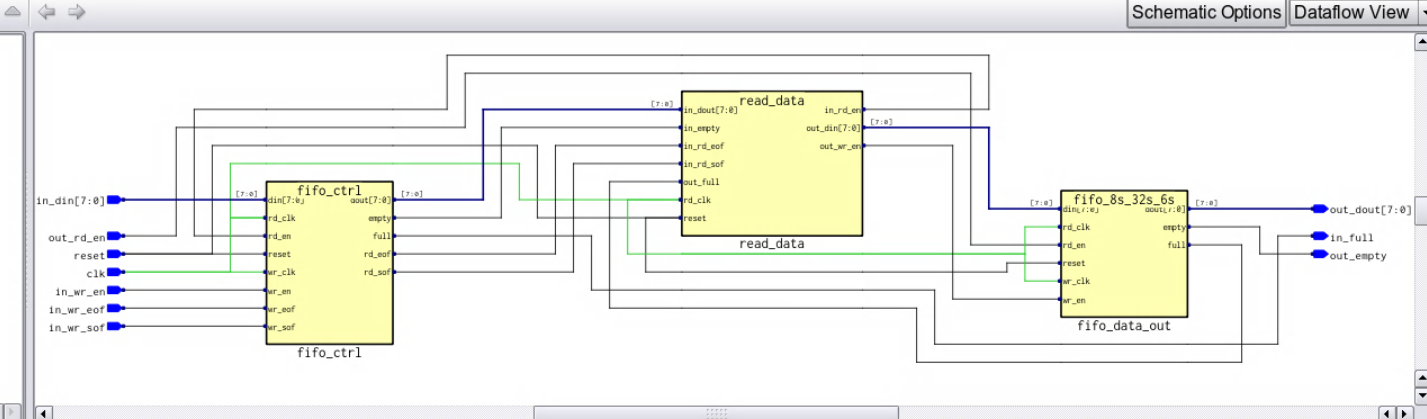
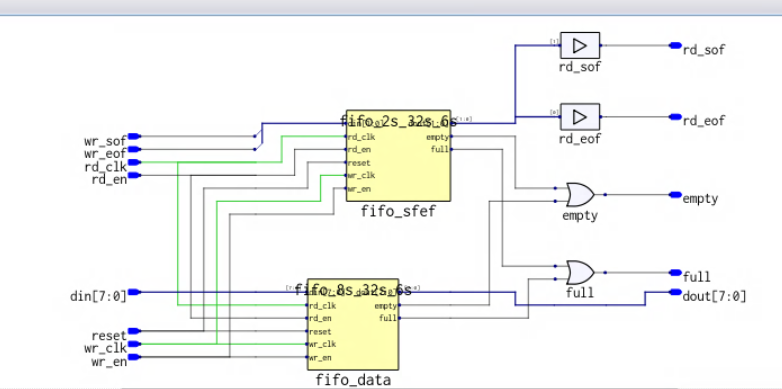
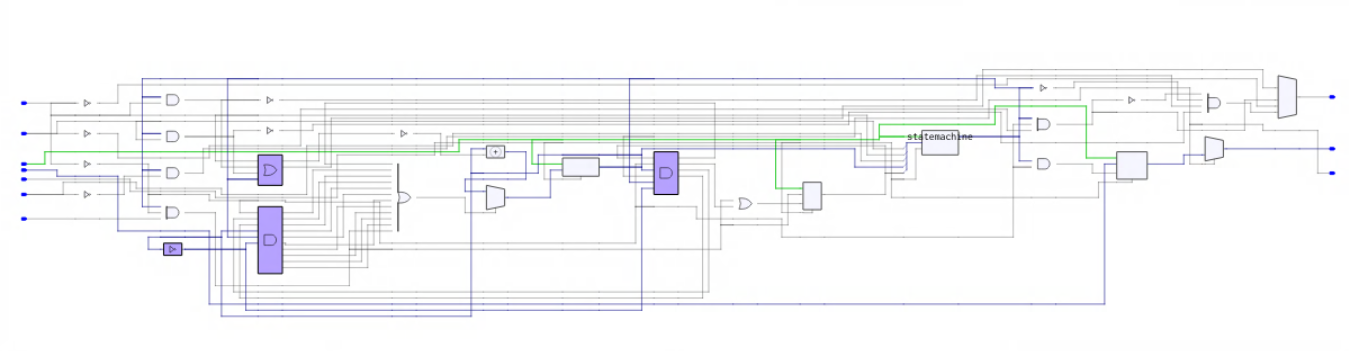
Clock period: 10ns

Running time 90205ns

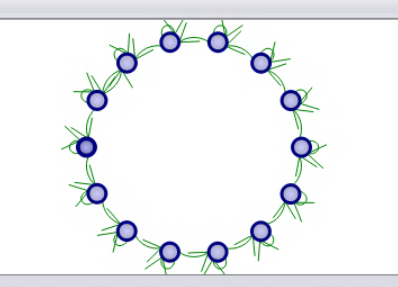
Throughput = 1/ time =11085 frames

overall structure

Ctrl fifo



Read data



FSM

##### START OF AREA REPORT #####[

Design view:work.udp\_top(verilog)

Selecting part EP4CE6E22A7

@N:FA174 : | The following device usage report estimates place and route data. Please look at the place and route report for final resource usage.

Total combinational functions 184 of 6272 ( 2%)

Logic element usage by number of inputs

4 input functions 87

3 input functions 30

[=2 input functions 67

Logic elements by mode

normal mode 150

arithmetic mode 34

Total registers 78 of 6272 ( 1%)

I/O pins 24 of 180 (13%), total I/O based on largest package of this part.

Number of I/O registers

Input DDRs :0

Output DDRs :0

DSP Blocks: 0 (0 nine-bit DSP elements).

DSP Utilization: 0.00% of available 15 blocks (30 nine-bit).

ShiftTap: 0 (0 registers)

Ena: 35

Sload: 0

Sclr: 16

Total ESB: 576 bits

##### END OF AREA REPORT #####]

##### START OF TIMING REPORT #####[

# Timing Report written on Mon Feb 19 09:38:37 2024

#

Top view: udp\_top

Requested Frequency: 214.9 MHz

Wire load mode: top

Paths requested: 5

Constraint File(s):

@N:MT320 : | This timing report is an estimate of place and route data. For final timing results, use the FPGA vendor place and route report.

@N:MT322 : | Clock constraints include only register-to-register paths associated with each individual clock.

Performance Summary

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Worst slack in design: -0.821

Requested Estimated Requested Estimated Clock Clock

Starting Clock Frequency Frequency Period Period Slack Type Group

------------------------------------------------------------------------------------------------------------------------

udp\_top|clk 214.9 MHz 182.7 MHz 4.653 5.474 -0.821 inferred Autoconstr\_clkgroup\_0

========================================================================================================================

Clock Relationships

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Clocks | rise to rise | fall to fall | rise to fall | fall to rise

-----------------------------------------------------------------------------------------------------------------

Starting Ending | constraint slack | constraint slack | constraint slack | constraint slack

-----------------------------------------------------------------------------------------------------------------

udp\_top|clk udp\_top|clk | 4.653 -0.821 | No paths - | No paths - | No paths -

=================================================================================================================

Note: 'No paths' indicates there are no paths in the design for that pair of clock edges.

'Diff grp' indicates that paths exist but the starting clock and ending clock are in different clock groups.

Interface Information

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

No IO constraint found

====================================

Detailed Report for Clock: udp\_top|clk

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Starting Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Arrival

Instance Reference Type Pin Net Time Slack

Clock

------------------------------------------------------------------------------------------------------------------------------------

fifo\_ctrl.fifo\_sfef.fifo\_buf udp\_top|clk synplicity\_altsyncram\_RAM\_R\_W\_1 q\_b[0] rd\_eof 4.154 -0.821

fifo\_ctrl.fifo\_sfef.fifo\_buf udp\_top|clk synplicity\_altsyncram\_RAM\_R\_W\_1 q\_b[1] rd\_sof 4.154 -0.503

read\_data.num\_bytes[0] udp\_top|clk dffeas q num\_bytes[0] 0.845 -0.448

read\_data.state[3] udp\_top|clk dffeas q state[3] 0.845 -0.353

read\_data.num\_bytes[6] udp\_top|clk dffeas q num\_bytes[6] 0.845 -0.285

read\_data.num\_bytes[4] udp\_top|clk dffeas q num\_bytes[4] 0.845 -0.279

read\_data.num\_bytes[14] udp\_top|clk dffeas q num\_bytes[14] 0.845 -0.279

read\_data.num\_bytes[11] udp\_top|clk dffeas q num\_bytes[11] 0.845 -0.273

read\_data.num\_bytes[5] udp\_top|clk dffeas q num\_bytes[5] 0.845 -0.271

read\_data.num\_bytes[10] udp\_top|clk dffeas q num\_bytes[10] 0.845 -0.271

====================================================================================================================================

Ending Points with Worst Slack

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Starting Required

Instance Reference Type Pin Net Time Slack

Clock

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read\_data.num\_bytes[0] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[1] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[2] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[3] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[4] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[5] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[6] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[7] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[8] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

read\_data.num\_bytes[9] udp\_top|clk dffeas sclr un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 4.657 -0.821

=========================================================================================================================

Worst Path Information

View Worst Path in Analyst

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Path information for path number 1:

Requested Period: 4.653

- Setup time: 0.609

+ Intrinsic clock delay: 0.613

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 4.657

- Propagation time: 5.478

- Clock delay at starting point: 0.000 (ideal)

= Slack (critical) : -0.821

Number of logic level(s): 2

Starting point: fifo\_ctrl.fifo\_sfef.fifo\_buf / q\_b[0]

Ending point: read\_data.num\_bytes[0] / sclr

The start point is clocked by udp\_top|clk [rising] on pin clock0

The end point is clocked by udp\_top|clk [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

------------------------------------------------------------------------------------------------------------------------------------------

fifo\_ctrl.fifo\_sfef.fifo\_buf synplicity\_altsyncram\_RAM\_R\_W\_1 q\_b[0] Out 4.154 4.154 -

rd\_eof Net - - 0.340 - 3

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb datad In - 4.494 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb combout Out 0.155 4.649 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 Net - - 0.326 - 1

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb datad In - 4.975 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb combout Out 0.155 5.130 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 Net - - 0.348 - 16

read\_data.num\_bytes[0] dffeas sclr In - 5.478 -

==========================================================================================================================================

Total path delay (propagation time + setup - ICD at endpoint) of 5.474 is 4.460(81.5%) logic and 1.014(18.5%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

Path information for path number 2:

Requested Period: 4.653

- Setup time: 0.609

+ Intrinsic clock delay: 0.613

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 4.657

- Propagation time: 5.478

- Clock delay at starting point: 0.000 (ideal)

= Slack (critical) : -0.821

Number of logic level(s): 2

Starting point: fifo\_ctrl.fifo\_sfef.fifo\_buf / q\_b[0]

Ending point: read\_data.num\_bytes[15] / sclr

The start point is clocked by udp\_top|clk [rising] on pin clock0

The end point is clocked by udp\_top|clk [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

------------------------------------------------------------------------------------------------------------------------------------------

fifo\_ctrl.fifo\_sfef.fifo\_buf synplicity\_altsyncram\_RAM\_R\_W\_1 q\_b[0] Out 4.154 4.154 -

rd\_eof Net - - 0.340 - 3

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb datad In - 4.494 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb combout Out 0.155 4.649 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 Net - - 0.326 - 1

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb datad In - 4.975 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb combout Out 0.155 5.130 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 Net - - 0.348 - 16

read\_data.num\_bytes[15] dffeas sclr In - 5.478 -

==========================================================================================================================================

Total path delay (propagation time + setup - ICD at endpoint) of 5.474 is 4.460(81.5%) logic and 1.014(18.5%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

Path information for path number 3:

Requested Period: 4.653

- Setup time: 0.609

+ Intrinsic clock delay: 0.613

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 4.657

- Propagation time: 5.478

- Clock delay at starting point: 0.000 (ideal)

= Slack (critical) : -0.821

Number of logic level(s): 2

Starting point: fifo\_ctrl.fifo\_sfef.fifo\_buf / q\_b[0]

Ending point: read\_data.num\_bytes[14] / sclr

The start point is clocked by udp\_top|clk [rising] on pin clock0

The end point is clocked by udp\_top|clk [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

------------------------------------------------------------------------------------------------------------------------------------------

fifo\_ctrl.fifo\_sfef.fifo\_buf synplicity\_altsyncram\_RAM\_R\_W\_1 q\_b[0] Out 4.154 4.154 -

rd\_eof Net - - 0.340 - 3

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb datad In - 4.494 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb combout Out 0.155 4.649 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 Net - - 0.326 - 1

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb datad In - 4.975 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb combout Out 0.155 5.130 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 Net - - 0.348 - 16

read\_data.num\_bytes[14] dffeas sclr In - 5.478 -

==========================================================================================================================================

Total path delay (propagation time + setup - ICD at endpoint) of 5.474 is 4.460(81.5%) logic and 1.014(18.5%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

Path information for path number 4:

Requested Period: 4.653

- Setup time: 0.609

+ Intrinsic clock delay: 0.613

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 4.657

- Propagation time: 5.478

- Clock delay at starting point: 0.000 (ideal)

= Slack (critical) : -0.821

Number of logic level(s): 2

Starting point: fifo\_ctrl.fifo\_sfef.fifo\_buf / q\_b[0]

Ending point: read\_data.num\_bytes[13] / sclr

The start point is clocked by udp\_top|clk [rising] on pin clock0

The end point is clocked by udp\_top|clk [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

------------------------------------------------------------------------------------------------------------------------------------------

fifo\_ctrl.fifo\_sfef.fifo\_buf synplicity\_altsyncram\_RAM\_R\_W\_1 q\_b[0] Out 4.154 4.154 -

rd\_eof Net - - 0.340 - 3

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb datad In - 4.494 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb combout Out 0.155 4.649 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 Net - - 0.326 - 1

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb datad In - 4.975 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb combout Out 0.155 5.130 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 Net - - 0.348 - 16

read\_data.num\_bytes[13] dffeas sclr In - 5.478 -

==========================================================================================================================================

Total path delay (propagation time + setup - ICD at endpoint) of 5.474 is 4.460(81.5%) logic and 1.014(18.5%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

Path information for path number 5:

Requested Period: 4.653

- Setup time: 0.609

+ Intrinsic clock delay: 0.613

+ Clock delay at ending point: 0.000 (ideal)

= Required time: 4.657

- Propagation time: 5.478

- Clock delay at starting point: 0.000 (ideal)

= Slack (critical) : -0.821

Number of logic level(s): 2

Starting point: fifo\_ctrl.fifo\_sfef.fifo\_buf / q\_b[0]

Ending point: read\_data.num\_bytes[12] / sclr

The start point is clocked by udp\_top|clk [rising] on pin clock0

The end point is clocked by udp\_top|clk [rising] on pin clk

Instance / Net Pin Pin Arrival No. of

Name Type Name Dir Delay Time Fan Out(s)

------------------------------------------------------------------------------------------------------------------------------------------

fifo\_ctrl.fifo\_sfef.fifo\_buf synplicity\_altsyncram\_RAM\_R\_W\_1 q\_b[0] Out 4.154 4.154 -

rd\_eof Net - - 0.340 - 3

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb datad In - 4.494 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 cycloneive\_lcell\_comb combout Out 0.155 4.649 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_a1 Net - - 0.326 - 1

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb datad In - 4.975 -

read\_data.un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 cycloneive\_lcell\_comb combout Out 0.155 5.130 -

un1\_next\_state\_0\_sqmuxa\_1\_0\_o2\_i\_1 Net - - 0.348 - 16

read\_data.num\_bytes[12] dffeas sclr In - 5.478 -

==========================================================================================================================================

Total path delay (propagation time + setup - ICD at endpoint) of 5.474 is 4.460(81.5%) logic and 1.014(18.5%) route.

Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value

##### END OF TIMING REPORT #####]